2017 IEEE Asian Solid-State Circuits Conference (A-SSCC)

November 6 - 8, 2017
Grand Hilton Hotel Seoul, Seoul, Korea

Sponsored by
IEEE Solid-State Circuits Society (IEEE SSCS)
# Advanced Program

## Contents

<table>
<thead>
<tr>
<th>Tutorial</th>
<th>1</th>
</tr>
</thead>
<tbody>
<tr>
<td>Plenary Speech 1</td>
<td>4</td>
</tr>
<tr>
<td>Plenary Speech 2</td>
<td>4</td>
</tr>
<tr>
<td>Session 2: A1L-A</td>
<td>6</td>
</tr>
<tr>
<td>Session 3: A1L-D</td>
<td>6</td>
</tr>
<tr>
<td>Session 4: A2L-A</td>
<td>7</td>
</tr>
<tr>
<td>Session 5: A2L-B</td>
<td>8</td>
</tr>
<tr>
<td>Session 6: A2L-C</td>
<td>8</td>
</tr>
<tr>
<td>Session 7: A2L-D</td>
<td>9</td>
</tr>
<tr>
<td>Session 8: Panel Discussion</td>
<td>10</td>
</tr>
<tr>
<td>Plenary Speech 3</td>
<td>11</td>
</tr>
<tr>
<td>Plenary Speech 4</td>
<td>11</td>
</tr>
<tr>
<td>Session 10: B1L-A</td>
<td>13</td>
</tr>
<tr>
<td>Session 11: B1L-B</td>
<td>13</td>
</tr>
<tr>
<td>Session 12: B1L-C</td>
<td>14</td>
</tr>
<tr>
<td>Session 13: B1L-D</td>
<td>15</td>
</tr>
<tr>
<td>Session 14: B2L-A</td>
<td>16</td>
</tr>
<tr>
<td>-------------------</td>
<td>----</td>
</tr>
<tr>
<td>Session 15: B2L-B</td>
<td>16</td>
</tr>
<tr>
<td>Session 16: B2L-C</td>
<td>17</td>
</tr>
<tr>
<td>Session 17: B2L-D</td>
<td>17</td>
</tr>
<tr>
<td>Session 18: B3L-A</td>
<td>18</td>
</tr>
<tr>
<td>Session 19: B3L-B</td>
<td>19</td>
</tr>
<tr>
<td>Session 20: B3L-C</td>
<td>19</td>
</tr>
<tr>
<td>Session 21: B3L-D</td>
<td>20</td>
</tr>
<tr>
<td>Tutorial 1</td>
<td>ADC hybrids and ADC morphing</td>
</tr>
<tr>
<td>------------</td>
<td>-------------------------------</td>
</tr>
<tr>
<td><strong>TUTORIAL</strong></td>
<td>09:00-10:30</td>
</tr>
<tr>
<td><strong>Tutorial 1</strong></td>
<td>Michael P. Flynn</td>
</tr>
<tr>
<td><strong>University of Michigan, USA</strong></td>
<td></td>
</tr>
</tbody>
</table>

**Biography**

Michael P. Flynn received the BE and the M.Eng.Sc degrees from UCC in Cork, Ireland in 1988 and 1990. He received the Ph.D. degree from Carnegie Mellon University in 1995. He was with National Semiconductor in Santa Clara, CA, from 1993 to 1995 and from 1995 to 1997 he was a Member of Technical Staff with Texas Instruments, Dallas, TX. During the four-year period from 1997 to 2001, he was with Parthus Technologies, Cork, Ireland. Dr. Flynn joined the University of Michigan in 2001 and is currently Professor. His technical interests are in data conversion, RF circuits, serial transceivers and biomedical systems. Michael Flynn is an IEEE Fellow and a 2008 Guggenheim Fellow. He was Editor-in-Chief of the IEEE Journal of Solid-State Circuits from 2013 to 2016.

**Abstract**

Hybrid ADC architectures combine existing architectures to improve the energy efficiency or performance of ADCs. Many hybrids take advantage of the energy efficiency of the SAR ADC architecture to make other architectures more efficient. For example, a SAR ADC can be used as a sub-ADC to improve energy efficiency or extend resolution of pipeline or sigma delta ADCs. Another hybrid approach noise-shapes the quantization and comparator noise in a SAR ADC. Extended counting ADCs combine sigma delta and Nyquist ADCs, which are often SAR ADCs, to achieve faster throughput. The zoom ADC is another hybrid between a sigma delta and a Nyquist ADC. At the same time hybridization blurs the boundaries between ADC architectures. Some new hybrids are simply other architectures wearing new clothes. This tutorial explores and categorizes hybrid ADCs, discusses the advantages of different hybrid architectures, and explains how sometimes hybridization really morphs one ADC type into another.

<table>
<thead>
<tr>
<th>Tutorial 2</th>
<th>Accelerator Design for Deep Learning Training</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Tutorial 2</strong></td>
<td>10:45-12:15</td>
</tr>
<tr>
<td><strong>Jinwook Oh</strong></td>
<td>IBM Research, USA</td>
</tr>
</tbody>
</table>

**Biography**

Jinwook Oh received the B.S. degree in EE from Seoul National University, South Korea, in 2008, and MS and the Ph.D. degrees in EE from Korea Advanced Institute of Science and Technology (KAIST), South Korea, in 2010 and 2013. In 2014, he joined IBM Thomas J. Watson Research Center, NY, USA as a research staff member of the accelerator architecture and machine learning team under the Science and Technology department of IBM Research. He has been working on developing new computing architecture designs for algorithms/applications running on IBM Watson and P/Z processors that includes machine learning, analytics and computer vision.

**Abstract**

Deep Neural Networks (DNNs) achieve superior accuracy for many applications with high computational complexity using very large models which require 100s of MBs of data storage, exaops of computation and high bandwidth for data movement. In spite of these impressive advances, it still takes days to weeks to train state of the art Deep Networks on large datasets. This
tutorial introduces a multi-pronged approach to address the challenges in meeting both the throughput and the energy efficiency goals for DNN training. It will incorporate a number of key features including the ability to support large-scale distributed DNN training tasks running on specialized (ASIC) hardware. Dataflow accelerators that support reduced precision computations and maintain high accelerator utilizations look promising as the industry looks to specialize beyond GPUs for Deep Learning.

Tutorial 3
Basics of Jitter in Wireline Communications
Ali Sheikholeslami
University of Toronto, Canada

Biography
Ali Sheikholeslami has been a professor at the University of Toronto, Canada, since 1999. His research interests are jitter, analog and digital integrated circuits, high-speed signaling, and memory design. He has published over 70 journal and conference articles including several on jitter. He has served as the ISSCC Education Chair since 2013, and as a member of its wireline committee from 2007 to 2013. Since 2016, he has been the Education Chair and the Distinguished Lecturer Program Chair for the Solid-State Circuits Society and an elected member of its Administration Committee. Prof. Sheikholeslami has received numerous teaching awards from the Faculty of Applied Science and Engineering at the University of Toronto. He is a co-author of a book entitled Understanding Jitter and Phase Noise, to appear in print by early 2018.

Abstract
Jitter refers to deviation from ideal timing in clock and data transitions. In wireline communications, jitter reduces the timing margin available for clock and data recovery (CDR) circuits and poses significant challenges to signal integrity as the data rates march towards 64Gb/s/lane and beyond.

In this tutorial, we first review the basic definitions of jitter and its properties, the relationship between jitter and phase noise, and the effects of jitter on CDR and other building blocks of a wireline system. We then describe the concept of jitter transfer, jitter generation, and jitter tolerance curves, and the methods of characterizing, modeling, and simulating jitter. Finally, we present some recent works on jitter measurement and jitter mitigation techniques that are used to optimize the link performance.

Tutorial 4
Emerging memory technology for IoT and AI applications
Takayuki Kawahara
Tokyo University of Science, Katsushika, Japan

Biography
Takayuki Kawahara is currently a Professor in the Department of Electrical Engineering at Tokyo University of Science, Katsushika, Japan. Sustainable electronics is the focus of his laboratory, which includes spin-current applications such as SOT-RAM. In the field of DRAM, his major contributions were low-voltage subthreshold-current reduction circuits. He also developed the world's first fully functional 2-Mb STT-RAM chip in 2007 and developed FD-SOI SRAM circuitry with back-gate control. From 1997 to 1998, he was a visiting researcher at the Swiss Federal Institute of Technology in Lausanne (EPFL). Prof. Kawahara is a recipient of the 9th (2009) Yamazaki-Teiichi Prize, the 2017 MEXT Commendation for Science and Technology, and he is an IEEE Fellow.

Abstract
We are enlightened through the progress of memory technology. It brings new materials and principles into the LSI field more frequently than any other technology. Moreover, commercial opportunities with considerable financial potential are possible.
Artificial intelligence (AI) and the Internet of Things (IoT) have been attracting attention. In this lecture, first, emerging memory devices such as phase-change RAM (PCRAM), magnetoresistive random-access memory (MRAM), resistive random-access memory (RRAM), and the status of large-scale integration are summarized. Typical spin-transfer torque (STT), spin-orbit torque (SOT), and voltage-controlled writing technologies are described in detail, especially with regard to MRAM. Next, prospective memories using examples for AI and IoT applications are shown in a
cloud/server area and in a things/edge area. The development trends of AI and IoT are also surveyed. Design challenges to make use of non-volatility are emphasized in each application. Finally, a new movement in which memory devices evolve from wearable to implantable is discussed.
## Plenary 1

### Technology Trends and Challenges in the Development of Future Automobiles

**Dr. Joseph Yoon**  
*Senior Vice President, Head of Vehicle Component Tech. Center, LG Electronics, Korea*

**Biography**

Joseph Yoon is Senior Vice President at LG Electronics and currently heading Vehicle Component Technology Center, CTO. Joseph is responsible for Advanced Research and development activities for all automotive related technologies. Joseph joined LG Electronics in 2015 after working in automotive industry in the United States for over 25 years and during his professional career, he has demonstrated a track record of success with increasing responsibilities in product development, manufacturing, technical sales, program management and Joint Venture. Joseph also has diverse experience in vehicle safety systems, Infotainment system, HVAC systems and Li-Ion battery manufacturing. Joseph is actively involved in community services including Soup Kitchen Charity organization. He also served as 30th President of KPAI (The Association of Korean Professionals in Automotive Industry), a non-profit organization (www.kpai.org) and founded a scholarship program in 2009 for the first time in KPAI's 30 year history in order to support students in financial needs and to help develop future leaders. Joseph earned his master’s degree in Aerospace Engineering from the University of Cincinnati and Bachelor of Science degree in Aeronautical Engineering from Seoul National University in Korea.

**Abstract**

With the success of electric cars, automotive system is considered the next generation platform for SoCs. And the market is moving rapidly to the next step, autonomous vehicle systems. In this talk, the history of SoCs and components in automotive systems and the requirements of SoCs for the next generation vehicles will be discussed with LG’s experiences and foresight.

## Plenary 2

### The Development of China's IC Industry - Its influence on global semiconductor community

**Dr. Prof. Shaojun Wei**  
*Dean of the Dept. of Micro- and Nano-Electronics, Tsinghua University, China Vice president, China Semiconductor Industry Association, China*

**Biography**

Prof. WEI received Master degree in Engineering from the Department of Radio and Electronics, Tsinghua University, Beijing, China in 1984 and Doctor degree in Applied Science in 1991 from the faculté Polytechnique de Mons (FPMs), Belgium and then became the assistant professor in FPMs. Dr. WEI returned to China in 1995. From 1998 to 2005, he worked for Datang Telecom Technology Co., Ltd. successively as Vice-President, President & CEO. He was the founder, President & CEO and Chairman of the Board of Datang Microelectronics Technology Co., Ltd. from 1996 to 2005. He was the CTO of Datang Telecom Industry Group from 2005 to 2006. Prof. WEI is the member of National IC Industry Advisory Committee, the Vice President of CSIA and President of VLSI fabless chapter. He is the fellow of CIE and senior member of IEEE. The research interests of Dr. WEI include VLSI design methodology and mobile computing and reconfigurable computing. He has published more than 190 papers in above area.
Prof. WEI has won many awards during last years, including the National 2nd Prize for Advanced Technology in 2002; the National 2nd Prize for Technology Invention in 2015; Beijing 1st and 2nd Prize for Advanced Technology in 2001 and 2004; the Award for Outstanding Chinese Patented Invention, State Intellectual Property Office of China & World Intellectual Property Organization in 2004 and 2015; the Outstanding Founder in Zhongguancun Science Park in 2001 and the Outstanding Leading Person in Semiconductor Industry, CSIA in 2003, etc.

Abstract

With the fast growing of its economy, China has become the largest IC market in the world since 2013. The huge number of IC imported each year makes both suppliers and buyers be fear. From the suppliers’ point of view, if China stopped to purchase IC that would be a catastrophe and from the buyers’ side, if the suppliers stopped to sell IC to China, that would lead to a disaster. That is the background for China to announce its national plan to promote its native IC industry. Inevitably, this raised many questions. For example, what is the real state of the China's IC industry today, what implications does such a promotion have to the global IC, EDA and other related industries, and what goals are China's IC industry working to achieve? Obviously, with its rapid growth, China's IC industry is becoming an emerging force globally, increasing the importance of understanding the answers to these questions. Unfortunately, few people really understand China's IC industry. This presentation will give an overview of the Chinese IC market, followed by an introduction of China's IC industry. China’s native products, design technologies, and talents will be described in detail to provide an objective and comprehensive picture of China's IC industry. As China is a unique country with huge population, vast territory, rapidly growing but unbalanced economy, and many diverse cultures, life-styles and traditions, its native product demands are also diverse. How to meet these drastically different requirements with a reasonable time to market while keeping costs low presents a big challenge. A rapidly growing IC industry in China will force engineers, both inside and outside China, to explore, to innovate as well as to collaborate. With a large talent pool addressing unique challenges, who can say there will not be new technologies, methodologies and products emerging to change the rules of the global information technology landscape?
### Session 2: A1L-A  Low-Power Programmable SoCs and Embedded Memories

**Chair 1:** Surhud Khare, Intel Corporation  
**Chair 2:** Daeyong Shim, SK Hynix  

**Convention Hall D (Convention Center 4F)**

<table>
<thead>
<tr>
<th>Session</th>
<th>Title</th>
<th>Presenters</th>
<th>Time</th>
</tr>
</thead>
</table>
| S2-1 (2027) | A Programmable RFSoC in 16nm FinFET Technology for Wideband Communications | Brendan Farley, Christophe Erdmann, Bruno Vaz, John McGrath, Edward Cullen, Bob Verbruggen, Roberto Pelliconi, Daire Breathnach, Peng Lim, Ali Boumaalif, Patrick Lynch, Conrado Mesadri, David Melinn, Kwee Peng Yap, and Liam Madden  
Xilinx Ireland, Dublin, Ireland | 10:45-11:10 |
| S2-2 (2166) | A Reconfigurable Analog Baseband Transformer for Multistandard Applications in 14nm FinFET CMOS | Jongmi Lee, Jongwoo Lee, Chilun Lo, Jaehoon Lee, In-Young Lee, Byungki Han, Seunghyun Oh, and Thomas Cho  
Samsung Electronics, Korea | 11:10-11:35 |
| S2-3 (2136) | A 1.4Mb 40-nm embedded ReRAM macro with 0.07um² bit cell, 2.7mA/100MHz low-power read and hybrid write verify for high endurance application | Chia-Fu Lee, Hon-Jarn Lin, Chiu-Wang Lien, Yu-Der Chih, and Jonathan Chang  
Taiwan Semiconductor Manufacturing Company, Taiwan | 11:35-12:00 |
| S2-4 (2045) | A Dynamic Power Reduction in Synchronous 2RW 8T Dual-Port SRAM by Adjusting Wordline Pulse Timing with Same/Different Row Access Mode | Yoshisato Yokoyama, Yuichiro Ishii, Haruyuki Okuda and Koji Nii  
Renesas Electronics Corporation, Tokyo, Japan | 12:00-12:25 |
| S2-5 (2067) | 14nm Broadwell Xeon® Processor family: Design methodologies and optimizations | Mahesh K Kumashikar, Shridhar G Bendi, Srikanth Nimmagadda, Anup J Deka, and Anil Agarwal  
Intel Corporation, Bangalore, India | 12:25-12:50 |

### Session 3: A1L-D  Circuits and Systems for Sensing and Security

**Chair 1:** Chung-Chih Hung, National Chiao Tung University  
**Chair 2:** Jun Deguchi, Toshiba Corp  

**Convention Hall E (Convention Center 4F)**

<table>
<thead>
<tr>
<th>Session</th>
<th>Title</th>
<th>Presenters</th>
<th>Time</th>
</tr>
</thead>
</table>
| S3-1 (2107) | A Dual-Axis MEMS Vibratory Gyroscope ASIC with 0.0061°/s/√Hz Noise Floor over 480 Hz Bandwidth | Zhichao Tan, Khiem Nguyen, Jeff Yan, Howard Samuels, Shane Keating, Paul Crocker and Bill Clark  
Analog Devices, Inc., USA | 10:45-11:10 |
S3-2 (2141) Chaos, Deterministic Non-Periodic Flow, for Chip-Package-Board Interactive PUF
Noriyuki Miura, Masanori Takahashi, Kazuki Nagatomo, and Makoto Nagata
Kobe University, Japan

S3-3 (2089) A 93μW 11Mbps Wireless Vital Signs Monitoring SoC with 3-Lead ECG, Bio-Impedance, and Body Temperature
Yuxuan Luo, Kok-Hin Teng, Yongfu Li, Wei Mao, Yong Lian, and Chun-Huat Heng
1National University of Singapore, Singapore
2York University, Canada

S3-4 (2090) A 16-Channel TDM Analog Front-end with Enhanced System CMRR for Wearable Dry EEG Recording
Tao Tang, Wang Ling Goh, Lei Yao, and Yuan Gao
1Nanyang Technological University, Singapore
2A*STAR, Singapore

S3-5 (2169) An Area-Efficient Amplifier-Less Digitally-Controlled Li-Ion Battery Charger in 0.35-μm CMOS
Sheng-Ying Lin and Tsung-Hsien Lin
National Taiwan University, Taiwan

Session 4: A2L-A Sensor Interface
Chair 1: Hao Yu, Nanyang Technological University
Chair 2: Tetsuya Hirose, Kobe University
Convention Hall D (Convention Center 4F)

S4-1 (2123) A 0.5V BJT-Based CMOS Thermal Sensor in 10-nm FinFET Technology
Da Shin Lin and Hao Ping Hong
1MediaTek, Taiwan
2MediaTek USA, USA

S4-2 (2138) An Ultra-low Power 169-nA 32.768-kHz Fractional-N PLL
Chun-Yu Lin, Tun-Ju Wang, Tzu-Hsuan Liu, and Tsung-Hsien Lin
National Taiwan University, Taiwan

S4-3 (2062) A 10kHz-BW 93.7dB-SNR Chopped ΔΣ ADC with 30V Input CM Range and 115dB CMRR at 10kHz
Long Xu, Johan H. Huijsing, and Kofi A.A. Makinwa
Delft University of Technology, The Netherlands

S4-4 (2143) An Energy-Efficient Self-Charged Crystal Oscillator with a Quadrature-Phase Shifter Technique
Wei-Sung Chang, Dai-En Jhou, Yu-Hong Yang, and Tai-Cheng Lee
National Taiwan University, Taiwan

S4-5 (2209) An Area-Efficient Capacitively-Coupled Sensor Readout Circuit with Current-Splitting
Session 5: A2L-B  Digital Building Blocks

**Chair 1:** Keiichi Kushida, Toshiba Corporation
**Chair 2:** Robert Chen-Hao Chang, National Chung Hsing University

<table>
<thead>
<tr>
<th>Paper</th>
<th>Title</th>
<th>Authors</th>
<th>Location</th>
</tr>
</thead>
<tbody>
<tr>
<td>S5-1 (2049)</td>
<td>25 fJ/bit, 5Mb/s, 0.3V True Random Number Generator With Capacitively-Coupled Chaos System and Dual-Edge Sampling Scheme</td>
<td>Anh Tuan Do and Xin Liu</td>
<td>Convention Hall B (Convention Center 4F)</td>
</tr>
<tr>
<td>S5-2 (2142)</td>
<td>A 1.25pJ/bit 0.048mm² AES Core with DPA Resistance for IoT Devices</td>
<td>Shengshuo Lu¹, Zhengya Zhang¹, Marios Papaefthymiou¹,²</td>
<td></td>
</tr>
<tr>
<td>S5-3 (2218)</td>
<td>A 0.40 pJ/cycle 981 μm² Voltage Scalable Digital Frequency Generator for SoC Clocking</td>
<td>Martin Cochet¹,², Sylvain Clerc³, Gu’enol’e Lallement¹,³, Fady Abouzeid³, Philippe Roche³, Jean-Luc Autran¹</td>
<td></td>
</tr>
<tr>
<td>S5-4 (2188)</td>
<td>A 10-GHz Multi-purpose Reconfigurable Built-in Self-Test Circuit for High-Speed Links</td>
<td>Myungguk Lee, Seungho Han, Jae-Yoon Sim, Hong-June Park, and Byungsub Kim</td>
<td></td>
</tr>
</tbody>
</table>

Session 6: A2L-C  PAM-4 Receiver Techniques

**Chair 1:** Wei-Zen Chen, National Chiao Tung University
**Chair 2:** Hayun Chung, Korea University

<table>
<thead>
<tr>
<th>Paper</th>
<th>Title</th>
<th>Authors</th>
<th>Location</th>
</tr>
</thead>
<tbody>
<tr>
<td>S6-1 (2103)</td>
<td>A 56Gbps PAM-4 Optical Receiver Front-end</td>
<td>Kuan-Lin Fu, and Shen-Iuan Liu</td>
<td>Convention Hall C (Convention Center 4F)</td>
</tr>
<tr>
<td>S6-2 (2129)</td>
<td>A Low-Power PAM4 Receiver Using 1/4-Rate Sampling Decoder with Adaptive Variable-Gain Rectification</td>
<td>Guang Zhu¹, Quan Pan¹, John Zhuang³, Charlie Zhi³, and C. Patrick Yue¹</td>
<td></td>
</tr>
<tr>
<td>S6-3 (2050)</td>
<td>A 82 mW 28 Gb/s PAM-4 Digital Sequence Decoder with built-in Error correction in 28nm FDSOI</td>
<td>Masum Hossain¹, Aurangozeb¹, AKM Delwar Hossain¹, and Maruf Mohammad²</td>
<td></td>
</tr>
</tbody>
</table>
A 51Gb/s, 320mW, PAM4 CDR with Baud-Rate Sampling for High-Speed Optical Interconnects

Nan Qi\textsuperscript{1,2}, Yuhang Kang\textsuperscript{1}, Qipeng Lin\textsuperscript{1}, Jianxu Ma\textsuperscript{3}, Jingbo Shi\textsuperscript{2}, Bozhi Yin\textsuperscript{7}, Chang Liu\textsuperscript{2}, Rui Bai\textsuperscript{2}, Shang Hu\textsuperscript{1}, Juncheng Wang\textsuperscript{2}, Jiangbing Du\textsuperscript{5}, Lin Ma\textsuperscript{5}, Zuyuan He\textsuperscript{5}, Ming Liu\textsuperscript{1}, Feng Zhang\textsuperscript{1}, and Patrick Yin Chiang\textsuperscript{2,6}

\textsuperscript{1}Chinese Academy of Sciences, China
\textsuperscript{2}Fudan University, China
\textsuperscript{3}PhotonIC Technologies, China
\textsuperscript{4}Shanghai Jiao Tong University, China.
\textsuperscript{5}Oregon State University, USA.

Session 7: A2L-D Building Blocks for Frequency Synthesizers

Chair 1: Davide Guermandi, IMEC
Chair 2: Minoru Fujishima, Hiroshima University

S7-1 (2052)
13:50-14:15
A 15-\textmu W, 103-fs step, 5-bit Capacitor-DAC-based Constant-Slope Digital-to-Time Converter in 28nm CMOS

Peng Chen\textsuperscript{1}, Feifei Zhang\textsuperscript{1}, Zhirui Zong\textsuperscript{1}, Hao Zheng\textsuperscript{1}, Teerachot Siriburanon\textsuperscript{1}, and Robert Bogdan Staszewski\textsuperscript{1}

\textsuperscript{1}University College Dublin, Ireland

S7-2 (2047)
14:15-14:40
A 173–200 GHz Quadrature Voltage-Controlled Oscillator in 130 nm SiGe BiCMOS

Paul Stärke, Vincent Rieß, Corrado Carta and Frank Ellinger

Technischen Universität Dresden, Germany

S7-3 (2025)
14:40-15:05
A 67 GHz Dual Injection Quadrature VCO with -182.9 dBc/Hz FOM in 90-nm CMOS

Cuei-Ling Hsieh, Hong-Shen Chen, Hou-Ru Pan, and Jenny Yi-Chun Liu

National Tsing Hua University, Taiwan

S7-4 (2174)
15:05-15:17
A 350-mV 2.4-GHz Quadrature Oscillator with Nearly Instantaneous Start-Up Using Series LC Tanks

Yue Chen\textsuperscript{1}, Masoud Babaie\textsuperscript{1}, and Robert Bogdan Staszewski\textsuperscript{1,2}

\textsuperscript{1}Delft University of Technology, The Netherlands
\textsuperscript{2}University College Dublin, Ireland

S7-5 (2046)
15:17-15:29
On-Chip Spur and Phase Noise Cancellation Techniques

Yi-An Li\textsuperscript{1}, Monte Mar\textsuperscript{2}, Borivoje Nikolić\textsuperscript{1}, Ali M. Niknejad\textsuperscript{1}

\textsuperscript{1}Berkeley Wireless Research Center (BWRC), University of California, USA
\textsuperscript{2}The Boeing Company, USA
### Session 8  
**Panel Discussion**  
Organizer: Junghwan Choi, Samsung  
Convention Hall A (Convention Center 4F)

<table>
<thead>
<tr>
<th>Time</th>
<th>Topic</th>
<th>Speaker</th>
</tr>
</thead>
<tbody>
<tr>
<td>16:00-17:40</td>
<td><strong>Future of Memory System and Technology</strong></td>
<td>Ken Takeuchi, Chuo University</td>
</tr>
<tr>
<td></td>
<td></td>
<td>1. Introduction : Ken Takeuchi (Chuo University)</td>
</tr>
<tr>
<td></td>
<td></td>
<td>2. 3D Stack : (Package) Tae Je Cho (Samsung Electro-Mechanics)</td>
</tr>
<tr>
<td></td>
<td></td>
<td>3. Circuits : (HBM) Daeyong Shim (SK Hynix)</td>
</tr>
<tr>
<td></td>
<td></td>
<td>4. Systems : (PIM) Meng-Fan Chang (National Tsing Hua University)</td>
</tr>
<tr>
<td></td>
<td></td>
<td>5. Applications : (AI and Big Data) Kihong Kim (SAP Korea VP)</td>
</tr>
<tr>
<td></td>
<td></td>
<td>6. Computer architecture : Mashubuchi (Toshiba)</td>
</tr>
</tbody>
</table>
# Plenary Speech

## November 8 (WED)

### Session 9  
**Plenary Speech**  

**Convention Hall A (Convention Center 4F)**

## Plenary 3: Robots, IoT, and AI for Smarter Manufacturing

<table>
<thead>
<tr>
<th>Time</th>
<th>Title</th>
<th>Speaker</th>
</tr>
</thead>
</table>
| 08:30-09:15 | Robots, IoT, and AI for Smarter Manufacturing | Dr. Shinsuke Sakakibara  
*Executive Director & Chief Technical Advisor,  
Robot Business Division, Fanuc Corporation, Japan* |

**Biography**

Dr. Shinsuke Sakakibara, received BE from Applied Physics Department, the University of Tokyo, in 1972, and joined FANUC. He has been serving as a manager of research and development group of intelligent robot at FANUC since 1985 and initiating the research and development of intelligent robot with vision and force sensors for assembly use. He received his doctoral degree in engineering from the University of Tokyo in 1995.

He has been serving as Honorary General Manager of Robot Laboratory at FANUC since 1999. He was appointed to President of RSJ, the Robotics Society of Japan, from 2009 to 2010. He was appointed to President of IFR, International Federation of Robotics, from 2012 to 2013. He has been serving as Executive Officer of FANUC since 2013. He has been serving as Executive Director & Chief Technical Advisor of FANUC since 2016.

**Abstract**

Robots are key for factory automation, such like Smart Manufacturing, and Industry 4.0. This Plenary talk covers introduction of the latest robot technologies and how they are being used for factory automation. The Plenary talk will cover "Collaborative Robots," which are attracting much attention in recent years for their ability to collaborate with humans, allowing both robots and humans to focus on the abilities that they excel at. Also, the Plenary Talk introduces examples of the use of the IoT and AI in factories that has been automated through the introduction of robots and outline recent trends involving an open platform that facilitates such applications.

## Plenary 4: Riding the Wave from Digital Consumer to Ubiquitous Intelligent Devices: Trends and Opportunities of IC Design

<table>
<thead>
<tr>
<th>Time</th>
<th>Title</th>
<th>Speaker</th>
</tr>
</thead>
</table>
| 09:15-10:00 | Riding the Wave from Digital Consumer to Ubiquitous Intelligent Devices: Trends and Opportunities of IC Design | Dr. Kou-Hung Lawrence Loh  
*Corporate Senior Vice President, MediaTek Inc.  
President, MediaTek USA Inc, USA* |

**Biography**

Dr. Kou-Hung Lawrence Loh is a Corporate Senior Vice President of MediaTek Inc. He oversees the company's Central Engineering Group, responsible for engineering the company's SOCs and chipsets design, development and implementation activities for all MediaTek's product lines including mobile communication, application processors, wireless connectivity, IOT, automotive, home entertainment, optical storage and broadband/networking business. He is also serving as President of MediaTek USA, Inc., responsible for the company's global operations in Europe and America.

Dr. Loh started his first circuit design position at IMP and later he joined Cirrus Logic, where his last position was Director of Analog IC Engineering. In 1998, he founded Silicon Bridge Inc., where he successfully led a number of analog/mixed-signal IC development projects with major
For the past decade, mobile consumer devices have predominantly driven CMOS technologies to continue to follow the path of Moore's Law. Today we are ready to enter the era of "Intelligent Device" which creates even more business opportunities for semiconductor companies. End products may contain essential sensory or control components such as for medical, automotive or other internet of things (IoT) applications. The resulting massive data flows have created strong demands of local 'intelligence' which requires end devices to perform respective computing and connecting functions at the lowest possible energy levels. In this plenary talk, technology trends of IC designs to bring up modern and future intelligent devices are presented from a SOC company's perspective. Innovations in development of underlying technologies including systems, algorithms, circuits, packaging and fabricating process technologies, become increasingly challenging yet essential to ride the wave into ubiquitous intelligent devices.
**Session 10: B1L-A**  
**Power management**

*Chair 1:* Takeshi Ueno, Toshiba Corporation  
*Chair 2:* Po-Chiun Huang, National Tsing Hua University  

**Convention Hall D (Convention Center 4F)**

**S10-1 (2057)**  
10:30-10:55  
**A Single-Inductor Triple-Input-Triple-Output (SITITO) Energy Harvesting Interface with Cycle-by-Cycle Source Tracking and Adaptive Peak-Inductor-Current Control**  
Chi-Wei Liu, Ming-Jie Chung, Hui-Hsuan Lee, Pei-Chun Liao, and Po-Hung Chen  
*National Chiao Tung University, Taiwan*

**S10-2 (2060)**  
10:55-11:20  
**An 88% Efficiency MPPT for PV Energy Harvesting System with Novel Switch Width Modulation for Output Power 100nW to 0.3mW**  
Karim Rawy, Taegeun Yoo and Tony T. Kim  
*Nanyang Technological University, Singapore*

**S10-3 (2122)**  
11:20-11:45  
**A DVS-Based Burst Mode with Automatic Entrance Point Control Technique in DC-DC Boost Converter for Wearable Devices and IoT Applications**  
Chiao-Hung Cheng¹, Li-Chi Lin¹, Jian-He Lin¹, Ke-Horng Chen¹, Ying-Hsi Lin², Jian-Ru Lin², and Tsung-Yen Tsai²  
¹National Chiao Tung University, Taiwan  
²Realtek Semiconductor Corp., Taiwan

**S10-4 (2086)**  
11:45-12:10  
**A Wide Load and Voltage Range Switched-Capacitor DC-DC Converter with Load-Dependent Configurability for DVS Implementation in Miniature Sensors**  
Hassan Saif, Yongmin Lee, Minsun Kim, Hyeonji Lee, Muhammad Bilawal Khan and Yoonmyung Lee  
*Sungkyunkwan University, Korea*

**S10-5 (2180)**  
12:10-12:35  
**A High Efficiency and Fast Transient Digital Low-Dropout Assisted Switched-Capacitor Converter for EMI-Free Internet of Everything (IoE) Systems**  
Shao-Qi Chen¹, Yen-Ting Lin¹, Yu-Sheng Ma², Wen-Hau Yang¹, Ke-Horng Chen¹, Ying-Hsi Lin², Jian-Ru Lin², and Tsung-Yen Tsai²  
¹National Chiao Tung University, Taiwan  
²Realtek Semiconductor Corporation, Taiwan

**Session 11: B1L-B**  
**Advanced Imaging System**

*Chair 1:* Youngcheol Chae, Yonsei University  
*Chair 2:* Jerald Yoo, National University of Singapore  

**Convention Hall B (Convention Center 4F)**

**S11-1 (2043)**  
10:30-10:55  
**A CMOS Time of Flight (TOF) Depth Image Sensor with In-Pixel Background Cancellation and Sensitivity Improvement Using Phase Shifting Readout Technique**
Ting Liao, Nien-An Lee, and Chih-Cheng Hsieh  
National Tsing Hua University, Taiwan

**S11-2 (2110)** 
**10:55-11:20**  
**An Element-Matched Band-Pass Delta-Sigma ADC for Ultrasound Imaging**  
Michele D’Urbino¹,², Chao Chen¹, Zhao Chen¹, Zu-Yao Chang¹, Jacco Ponte³, and Michiel Pertijs¹  
¹Delft University of Technology, The Netherlands  
²Oldelft Ultrasound, The Netherlands  
³Caeleste CVBA, Belgium

**S11-3 (2190)**  
**11:20-11:45**  
**A 12.1mW, 60dB SNR, 8-Channel Beamforming Embedded SAR ADC for Ultrasound Imaging Systems**  
Taehoon Kim and Suhwan Kim  
Seoul National University, Korea

**S11-4 (2207)**  
**11:45-12:10**  
**A 2.79-mW 0.5%-THD CMOS Current Driver IC for Portable Electrical Impedance Tomography System**  
Jaeeun Jang¹, Minseo Kim¹, Joonsung Bae² and Hoi-Jun Yoo¹  
¹Korea Advanced Institute of Science and Technology (KAIST), Korea  
²Kangwon National University, Korea

**S11-5 (2186)**  
**12:10-12:35**  
**0.5 and 1.5 THz Monolithic Imagers in a 65 nm CMOS Adopting a VCO-Based Signal Processing**  
Suna Kim, Kyoung-Yong Choi, Dae-Woong Park, Joo-Myoung Kim, Seok-Kyun Han, and Sang-Gug Lee  
Korea Advanced Institute of Science and Technology (KAIST), Korea

---

**Session 12: B1L-C Memory System**  
*Chair 1: Kazutaka Miyano, Micron*  
*Chair 2: Ik Joon Chang, Kyunghee University*  
*Convention Hall C (Convention Center 4F)*

**S12-1 (2009)**  
**10:30-10:55**  
**Dual-Loop 2-step ZQ Calibration for Dedicated Power Supply Voltage in LPDDR4 SDRAM**  
Samsung Electronics, Korea

**S12-2 (2224)**  
**10:55-11:20**  
**MLC/3LC NAND Flash SSD Cache with Asymmetric Error Reduction Huffman Coding for Tiered Hierarchical Storage**  
Hikaru Watanabe, Yoshiaki Deguchi and Ken Takeuchi  
Chuo University, Japan

**S12-3 (2175)**  
**11:20-11:45**  
**Word-line Batch $V_{TH}$ Modulation of TLC NAND Flash Memories for Both Write-Hot and Cold Data**  
Yoshiaki Deguchi and Ken Takeuchi  
Chuo University, Japan
A 16kb Column-based Split Cell-VSS, Data-Aware Write-Assisted 9T Ultra-Low Voltage SRAM with Enhanced Read Sensing Margin in 28nm FDSOI
M. Sultan M. Siddiqui, Zhao Chuan Lee, and Tony Tae-Hyoung Kim
Nanyang Technological University, Singapore

An Energy-optimized (37840, 34320) Symmetric BC-BCH Decoder for Healthy Mobile Storages
Seokha Hwang¹, Jaehwan Jung², Daesung Kim³, Jeongseok Ha², In-Cheol Park² and Youngjoo Lee⁴
¹Kwangwoon University, Korea
²Korea Advanced Institute of Science and Technology (KAIST), Korea
³SK Hynix, Korea
⁴Pohang University of Science and Technology (POSTECH), Korea

A 130nm 1Mb HfO₂ Embedded RRAM Macro Using Self-Adaptive Peripheral Circuit System Techniques for 1.6X Work Temperature Range
Feng Zhang¹, Dongyu Fan¹,², Yuan Duan¹, Jin Li¹, Cong Fang¹, Yun Li¹, Xiaowei Han³, Lan Dai², Chengying Chen¹, Jinshun Bi¹, Ming Liu¹, and Meng-Fan Chang⁴
¹Institute of Microelectronics Chinese Academy of Sciences, China
²North China University of Technology, China
³Xi'an UniIC Semiconductors Co., Ltd., China
⁴National Tsing Hua University, Taiwan

Session 13: B1L-D Wireless Receivers and Transmitters
Chair 1: Tae Wook Kim, Yonsei University
Chair 2: Chien-Nan Kuo, National Chiao Tung University
Convention Hall E (Convention Center 4F)

A Reconfigurable Dual-Band WiFi/BT Combo Transceiver with Integrated 2G/BT SP3T, LNA/PA Achieving Concurrent Receiving and Wide Dynamic Range Transmitting in 40nm CMOS
Meng-Hsiung Hung, Yi-Shing Shih, Chin-Fu Li, Wei-Kai Hong, Ming-Yeh Hsu, Chih-Hao Chen, Yu-Lun Chen, Chun-Wei Lin, and Yuan-Hung Chung
MediaTek Inc, Taiwan

A High-Speed DDFS MMIC with Frequency, Phase and Amplitude Modulations in 65nm CMOS
Abdel Martinez Alonso, Masaya Miyahara, and Akira Matsuzawa
Tokyo Institute of Technology, Japan

A ~121dBm Sensitivity, 2.8μJ/bit Rx, 8.8μJ/bit Tx, Narrowband transceiver for ARIB STD and IoT
M. Kumarasamy Raja, Zhao Bin, Yan Dan Lei, Zhang Hongbao, Lim Wei Yi, and Chemmanda John Leo
A*STAR (Agency for Science, Technology and Research), Singapore

Detection of 3.0 THz wave with a detector in 65 nm standard CMOS process
Tong Fang, Zhao-yang Liu, Li-yuan Liu, Yuan-yuan Li, Jun-qi Liu, Jian Liu, and Nan-jian Wu
University of Chinese Academy of Sciences, China
S13-5 (2217)  A 0.6-V 200-kbps 429-MHz Ultra-low-power FSK Transceiver in 90-nm CMOS
12:10-12:35  Chun-Yuan Chiu, Zhen-Cheng Zhang, and Tsung-Hsien Lin
National Taiwan University, Taiwan

Session 14: B2L-A  Energy-efficient & Variation resilient Digital Circuits
Chair 1: Mototsugu Hamada, Keio University
Chair 2: Yoonmyung Lee, Sungkyunkwan University
Convention Hall D (Convention Center 4F)

S13-1 (2028)  An 82% Energy-Saving Change-Sensing Flip-Flop in 40nm CMOS for Ultra-Low Power Applications
13:40-14:05  Van Loi Le1,2, Juhui Li2, Alan Chang2, and Tony T. Kim1
1Nanyang Technological University, Singapore
2NXP Semiconductors, Singapore

S13-2 (2150)  NBTI/PBTI separated BTI monitor with 4.2x Sensitivity by Standard Cell Based Unbalanced Ring Oscillator
14:05-14:30  Mitsuhiro Igarashi, Yoshio Takazawa, Yasumasa Tsukamoto, Kan Takeuchi, and Koji Shibutani
Renesas Electronics Corporation, Japan

S13-3 (2034)  A 0.44V-1.1V 9-Transistor Transition-Detector and Half-Path Error Detection Technique for Low Power Applications
14:30-14:55  Xinchao Shang, Weiwei Shan, Longxing Shi, Xing Wan, and Jun Yang
Southeast University, China

S13-4 (2155)  HTD: A Light-Weight Holosymmetrical Transition Detector Based In-situ Timing Monitoring Technique for Wide-Voltage-Range in 40nm CMOS
14:55-15:20  Wentao Dai, Weiwei Shan, Xinning Liu, and Jun Yang
Southeast University, China

Session 15: B2L-B  Nyquist-rate ADCs
Chair 1: Seung-Tak Ryu, KAIST
Chair 2: Yan Zhu, University of Macau
Convention Hall B (Convention Center 4F)

S15-1 (2133)  A 0.5V 12-bit SAR ADC using Adaptive Time-Domain Comparator with Noise Optimization
13:40-14:05  Chen-Che Kao, Sung-En Hsieh, and Chih-Cheng Hsieh
National Tsing Hua University, Taiwan

S15-2 (2203)  Range Pre-selection Sampling technique to reduce input drive energy for SAR ADCs
14:05-14:30  Harjot Singh Bindra1, Joeri Lechevallier1, Anne-Johan Annema2, Simon Louwsma2, Ed van Tuijl1,2, and Bram Nauta1
1University of Twente, The Netherlands
2Teledyne DALSA, The Netherlands

S15-3 (2064)  A 5-bit 2 GS/s Binary-Search ADC with Charge-Steering Comparators
14:30-14:55  U-Fat Chio, Sai-Weng Sin1, Seng-Pan U1,2, Franco Maloberti3, and R. P. Martins1,4
1University of Macau, Macao, China
A 13-bit 160MS/s Pipelined Subranging-SAR ADC with Low-Offset Dynamic Comparator
Weitao Li, Fule Li, Jia Liu, Hongyu Li, and Zhihua Wang
Tsinghua university, China

A 1.5fJ/Conv-step 10b 100kS/s SAR ADC with Gain-Boosted Dynamic Comparator
Xiyuan Tang, Long Chen, Jeonggoo Song, and Nan Sun
The University of Texas at Austin, USA

Session 16: B2L-C Machine Learning and Recognition SoCs
Chair 1: Byeong-Gyu Nam, Chungnam National University
Chair 2: Tsung-Te Liu, National Taiwan University
Convention Hall C (Convention Center 4F)

A 2.56mm² 718GOPS Configurable Spiking Convolutional Sparse Coding Processor in 40nm CMOS
Chester Liu, Sung-Gun Cho, and Zhengya Zhang
University of Michigan, USA

A 21mW Low-power Recurrent Neural Network Accelerator with Quantization Tables for Embedded Deep Learning Applications
Jinmook Lee, Dongjoo Shin, and Hoi-Jun Yoo
Korea Advanced Institute of Science and Technology (KAIST), Korea

EQSCALE: Energy-Quality Scalable Feature Extraction Engine for Sub-mW Real-time Video Processing with 0.55 mm² Area in 40nm CMOS
Anastacia B. Alvarez2, Gopalakrishnan Ponnumam3, and Massimo Alioto1
1National University of Singapore, Singapore
2University of the Philippines, Philippines

A Self-Powered Always-On Vision-based Wake-up Detector for Wearable Gesture User Interfaces
Suhwan Cho, Seongrim Choi, Junsik Woo, Ara Kim, and Byeong-Gyu Nam
Chungnam National University, Korea

Session 17: B2L-D Advanced Wireline Clock Generators and Transmitters
Chair 1: Jung-Hoon Chun, Sungkyunkwan University
Chair 2: Ziqiang Wang, Tsinghua University
Convention Hall E (Convention Center 4F)

A 18-to-23 GHz -253.5dB-FoM Sub-Harmonically Injection-Locked ADPLL with ILFD Aided Adaptive Injection Timing Alignment Technique
Zhao Zhang, Jincheng Yang, Liyuan Liu, Peng Feng, Jian Liu, and Nanjian Wu
University of Chinese Academy of Sciences, China
### Session 17: S17-1 (2115)

**14:05-14:30**

**A 1.5-GHz Sub-Sampling Fractional-N PLL for Spread-Spectrum Clock Generator in 0.18-μm CMOS**

Chun-Yu Lin, Tun-Ju Wang, and Tsung-Hsien Lin  
*National Taiwan University, Taiwan*

---

### Session 17: S17-2 (2191)

**14:30-14:55**

**A 2.1Gbps 12-Channel Transmitter with Phase Emphasis Embedded Serializer for UHD Intra-panel Interface**

Jihwan Park, Joo-Hyung Chae, Yong-Un Jeong, Jae-Whan Lee, and Suhwan Kim  
*Seoul National University, Korea*

---

### Session 17: S17-3 (2099)

**14:55-15:20**

**A Low-Power Dual-Mode 20-Gb/s NRZ and 28-Gb/s PAM-4 Voltage-Mode Transmitter**

Hae-Woong Yang\(^1\), Ashkan Roshan-Zamir\(^1\), Young-Hoon Song\(^2\), and Samuel Palermo\(^1\)  
\(^1\)Texas A&M University, USA  
\(^2\)NXP Semiconductor, USA

---

## Session 18: B3L-A Analog Techniques

*Chair 1: Po-Hung Po-Hung, National Chiao Tung University*  
*Chair 2: Hyun-Sik Kim, Dankook University*  
*Convention Hall D (Convention Center 4F)*

### Session 18: S18-1 (2117)

**15:50-16:15**

**Subthreshold Voltage Reference With Nwell/Psub Diode Leakage Compensation for Low-Power High-Temperature Systems**

Inhee Lee, Dennis Sylvester, and David Blaauw  
*University of Michigan, USA*

### Session 18: S18-2 (2192)

**16:15-16:40**

**A Smart-Offset Analog LDO with 0.3V Minimum Input Voltage and 99.1% Current Efficiency**

Saurabh Chaubey and Ramesh Harjani  
*University of Minnesota, USA*

### Session 18: S18-3 (2151)

**16:40-17:05**

**A 762-μW 16.3-ps Resolution Digital Pulse Width Modulator Using Zooming Phase-Interpolator**

Masanobu Tsuji  
*ROHM Co., Ltd., Japan*

### Session 18: S18-4 (2157)

**17:05-17:29**

**Fully-Integrated AMLED Micro Display System With a Hybrid Voltage Regulator**

Junmin Jiang, Liusheng Sun, Xu Zhang, Shing Hin Yuen, Xianbo Li, Wing-Hung Ki, C. Patrick Yue, and Kei May Lau  
*The Hong Kong University of Science and Technology, Hong Kong*

### Session 18: S18-4 (2197)

**17:17-17:29**

**A Low-Voltage Low-Offset Dual Strong-Arm Latch Comparator**

Aikaterini Papadopoulou\(^1\), Vladimir Milovanović\(^2\), and Borivoje Nikolić\(^1\)  
\(^1\)University of California at Berkeley, USA  
\(^2\)University of Kragujevac, Serbia
### Session 19: B3L-B

**High-resolution ADCs**

*Chair 1: Liyuan Liu, Chinese Academy of Sciences*
*Chair 2: Shanthi Pavan, Indian Institute of Technology, Madras*

**Convention Hall B (Convention Center 4F)**

#### S19-1 (2032)

**A 5.35 mW 10 MHz Bandwidth CT Third-Order ΔΣ Modulator with Single Opamp Achieving 79.6/84.5 dB SNDR/DR in 65 nm CMOS**

Wei Wang, Yan Zhu, Chi-Hang Chan, Seng-Pan U, and Rui Paulo Martins

1. University of Macau, Macao, China
2. Synopsys Macau Ltd., Macao, China
3. Instituto Superior Técnico/Universidade de Lisboa, Portugal

**Time:** 15:50-16:15

#### S19-2 (2120)

**A 72.9-dB SNDR 20-MHz BW 2-2 Discrete-Time Sturdy MASH Delta-Sigma Modulator Using Source-Follower-Based Integrators**

Yong-Sik Kwak, Kang-Il Cho, Ho-Jin Kim, Seung-Hoon Lee, and Gil-Cho Ahn

Sogang University, Korea

**Time:** 16:15-16:40

#### S19-3 (2042)

**A Compact 87.1-dB DR Bandwidth-Scalable Delta-Sigma Modulator Based on Dynamic Gain-Bandwidth-Boosting Inverter for Audio Applications**

Young-Ha Hwang, Jun-Eun Park, and Deog-Kyoon Jeong

Seoul National University, Korea

**Time:** 16:40-17:05

#### S19-4 (2176)

**A 172dB-FoM Pipelined SAR ADC Using a Regenerative Amplifier with Self-Timed Gain Control and Mixed-Signal Background Calibration**

Miguel Gandara, Paridhi Gulati, and Nan Sun

1. The University of Texas at Austin, USA
2. Analog Devices, Inc., USA

**Time:** 17:05-17:30

### Session 20: B3L-C

**IPs for Emerging Applications**

*Chair 1: Chun Zhang, Tsinghua University*
*Chair 2: Pei-Yun Tsai, National Central University*

**Convention Hall C (Convention Center 4F)**

#### S20-1 (2016)

**A Fully-Synthesizable C-Element Based PUF Featuring Temperature Variation Compensation with Native 2.8% BER, 1.02fJ/b at 0.8-1.0V in 40nm**

Sachin Taneja, Anastacia Alvarez, Gopalakrishnan Sadagopan, and Massimo Alioto

National University of Singapore, Singapore

**Time:** 15:50-16:15

#### S20-2 (2202)

**A 0.37mm² LTE/Wi-Fi Compatible, Memory-Based, Runtime-Reconfigurable 2²³m⁵¹ FFT Accelerator Integrated with a RISC-V Core in 16nm FinFET**

Angie Wang, Brian Richards, Palmer Dabbelt, Howard Mao, Stevo Bailey, Jaeduk Han, Eric Chang, James Dunn, Elad Alon, and Borivoje Nikolić

University of California, USA

**Time:** 16:15-16:40

#### S20-3 (2200)

**A 65nm 376nA 0.4V Linear Classifier Using Time-Based Matrix-Multiplying ADC with Non-Linearity Aware Training**

Anvesha A and Arijit Raychowdhury

Georgia Institute of Technology, USA

**Time:** 16:40-17:05

#### S20-4 (2167)

**A 1GHz Fault Tolerant Processor with Dynamic Lockstep and Self-recovering Cache for ADAS SoC Complying with ISO26262 in Automotive Electronics**

**Time:** 17:05-17:30
Jinho Han\textsuperscript{1,2}, Youngsu Kwon\textsuperscript{1}, Yong Cheol Peter Cho\textsuperscript{1}, and Hoi-Jun Yoo\textsuperscript{2}
\textsuperscript{1}Electronics and Telecommunications Research Institute (ETRI), Korea
\textsuperscript{2}Korea Advanced Institute of Science and Technology (KAIST), Korea

**Session 21: B3L-D**

**High performance RF Frequency generation Techniques**

*Chair 1*: Minjae Lee, Gwangju Institute of Science and Technology
*Chair 2*: Taizo Yamawaki, Hitachi

**S21-1 (2194)** A 77-GHz Mixed-Mode FMCW Signal Generator Based on Bang-Bang Phase Detector
Jianfu Lin\textsuperscript{1}, Zheng Song\textsuperscript{1}, Nan Qi\textsuperscript{2}, Woogeun Rhee\textsuperscript{1}, and Baoyong Chi\textsuperscript{1}
\textsuperscript{1}Tsinghua University, China
\textsuperscript{2}Chinese Academy of Sciences, China

**S21-2 (2125)** A 7GHz-Bandwidth 31.5 GHz FMCW-PLL with Novel Twin-VCOs Structure in 65nm CMOS
Shunli Ma, Jili Sheng, Ning Li, and Junyan Ren
Fudan University, China

**S21-3 (2071)** A -245 dB FOM 48 fs rms jitter semi-digital PLL with intrinsic temperature compensation in 130 nm CMOS
J. Anders\textsuperscript{1}, S. Bader\textsuperscript{1}, M. Dietl\textsuperscript{2}, P. Sareen\textsuperscript{2}, G. Rombach\textsuperscript{2}, S. Tambouris\textsuperscript{2}, and M. Ortmanns\textsuperscript{1}
\textsuperscript{1}University of Ulm, Germany
\textsuperscript{2}Texas Instruments Germany, Germany

**S21-4 (2080)** An Ultra-Low Phase Noise All-Digital Multi-Frequency Generator Using Injection-Locked DCOs and Time-Interleaved Calibration
Suneui Park, Heein Yoon, and Jaehyouk Choi
Ulsan national Institute of Science and Technology (UNIST), Korea